

Class	Subclass
	1

ISSUE CLASSIFICATION

PATENT NUMBER

## U.S. UTILITY Patent Application

<p>RP</p> <p>SCANNED</p>	<p>O.I.P.E.</p> <p>157</p> <p>QA</p>	<p>PATENT DATE</p> <p>170</p>
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APPLICATION NO. 097649437	CONT/PRIOR 097649437	CLASS 214 23 7#	SUBCLASS 200	ART UNIT 213 2187	EXAMINER H. J. [Signature]
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## APPLICANTS

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## ଆମ୍ଭ

Method and apparatus for specifying addressability and bus connections in a logic design C

PTO-2040  
12/89

**ISSUING CLASSIFICATION**

[illegible]

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.				<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____					
				<b>ISSUE FEE</b>	
				Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.				<b>ISSUE BATCH NUMBER</b>	

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